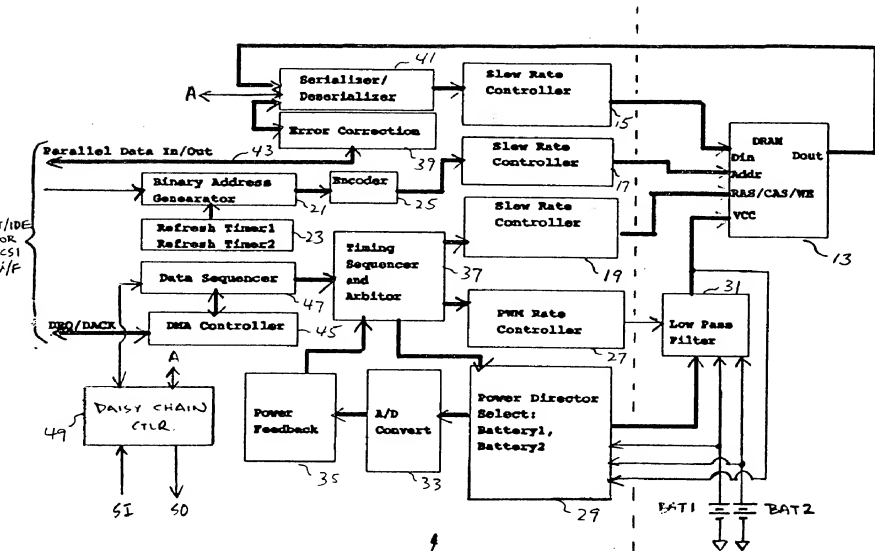


Figure 1



Power Sequence

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+5V
 +3V
 +2V
 +1.5V

RAM VCC

Fig 2a

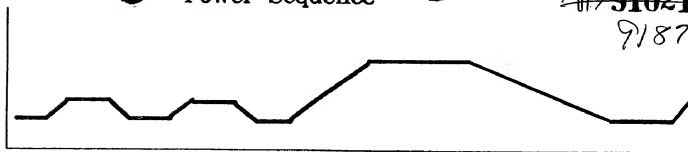


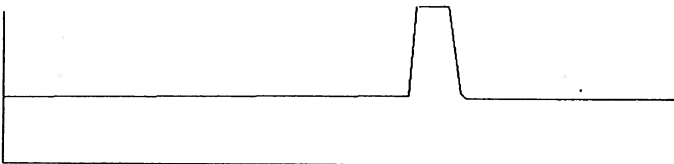
Fig 2b

Standby	Prepare Refresh	Refresh	Prepare Standby	Standby
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Fig 2c



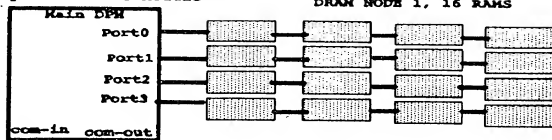
Fig 2d



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Dynamic Power Module

DRAM NODE 1, 16 RAMS



DRAM NODE 2, 16 RAMS

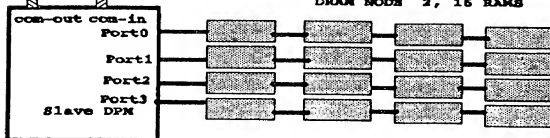


Fig 3

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Voltage across DRAMS For Four DRAMS

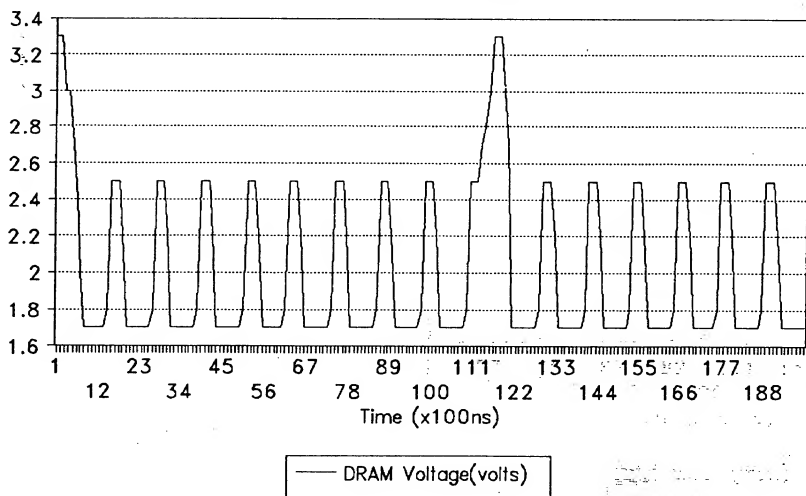


Fig 4

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Power for Four Rams over one Period (Refresh access is included)

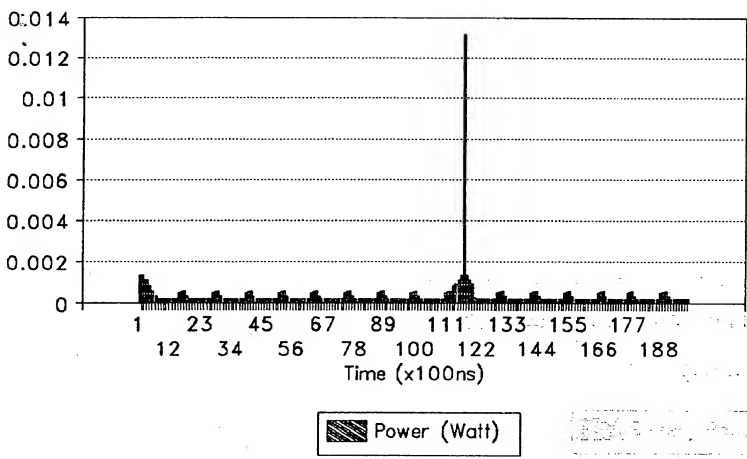


Fig 5

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Battery Power Consumed For Four DRAMs

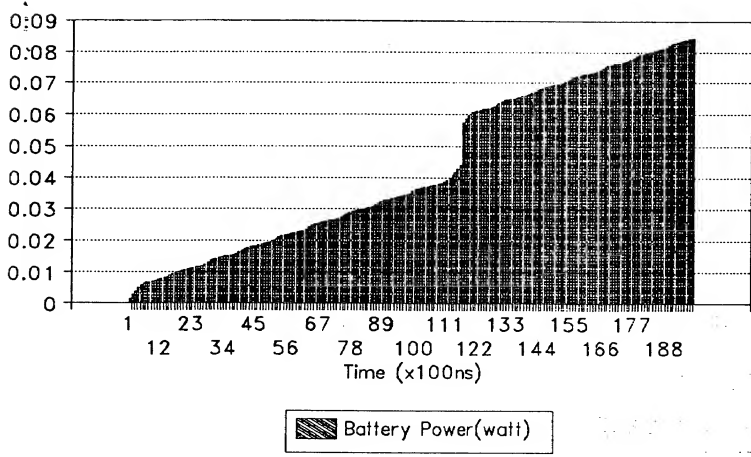


Fig 6

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Battery Life(50mAHr), 8 DRAMS (Hot Standby Battery)

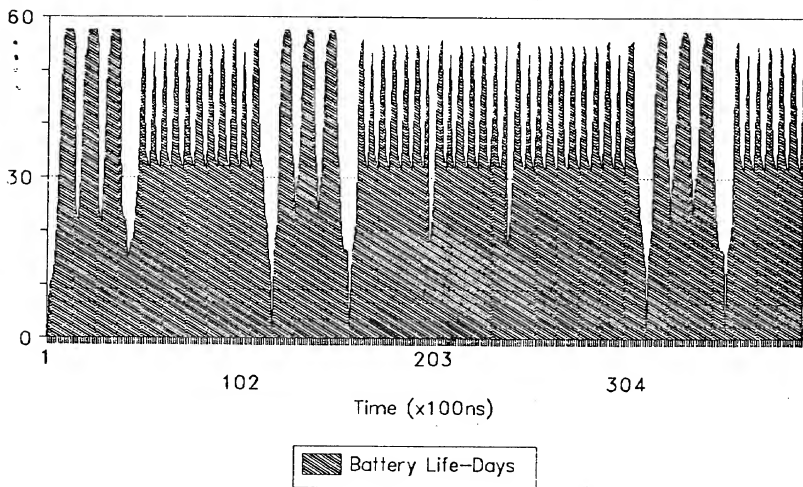


Fig 7